CAPACITIVELY COUPLED TRAVELING-WAVE POWER AMPLIFIER

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ABSTRACT

A new circuit concept which significantly improves the power-handling capability of a traveling-wave amplifier by coupling the active devices to the input gate line through discrete series capacitors is described. The approach is applied to a 2-8 GHz monolithic amplifier design.

Introduction

In distributed or traveling-wave amplifiers there are mechanisms which limit the output power [1]. In this paper, we present a new circuit concept which significantly improves the power-handling capability of a traveling-wave amplifier by coupling the active devices to the input gate line through discrete series capacitors. Combined with the gate-source capacitance of the FETs, these capacitors act as potential dividers, allowing us to sample a desired portion of the input signal from the gate line. In addition, by varying the divider ratio along the gate line, it is possible to tailor the input excitation to individual FETs. In this manner the input power can be increased significantly (typically by a factor of four) and the total device periphery can be at least doubled. This results in increased power output and efficiency.

The concept of capacitively coupling the individual FETs to the input gate line in a traveling-wave amplifier is illustrated in Fig. 1. Discrete thin-film capacitors are inserted in series with the FET gate terminals. If we approximate the input impedance of the FET by its gate capacitance,

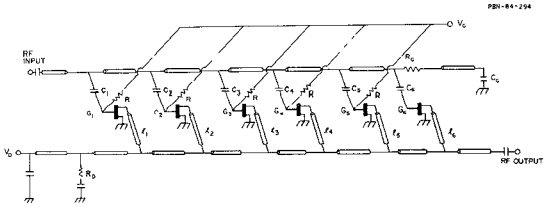

Fig. 1. Schematic circuit diagram of capacitively coupled traveling-wave amplifier.

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it is clear that we are forming a capacitive potential divider and only a portion of the rf voltage excited in the input line will appear at the gate of the discrete FETs. This voltage division will be independent of frequency. Fig. 2 shows the simplified equivalent circuit diagram for the first cell.

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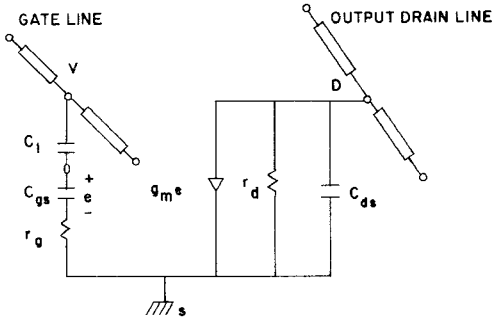

Fig. 2. The first cell of Fig. 1.

From this figure, it is clear that when $\omega C_{gs} r_g << 1$, the equivalent capacitance loading the gate line is

$$C_g = \frac{C_1 C_{gs}}{C_1 + C_{gs}}$$

and the voltage drop across the gate junction is

$$e = \frac{C_1}{C_1 + C_{gs}} \quad V$$

For example, if $C_1 = C_{gs}$, then

$$C_g = C_{gs}/2$$

$$e = \frac{V}{2}$$

The reduction in the voltage across the gate junction will result in this case in 6 dB gain reduction for the overall amplifier. However, this can be compensated by doubling both the periphery of the FETs and the value of C_1. Although it does not look like we have gained anything, this new circuit configuration accomplishes the following:

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1. The capacitors in series with the FET gate-source capacitance act as capacitive voltage dividers, reducing the magnitude of the rf voltage swing at the gate terminal. A reduction in voltage by half corresponds to a fourfold increase in input power-handling capability.

2. To achieve the same gain per stage, the periphery of each device should be doubled. The increased gate periphery does not increase the gate line loading. Hence, this approach allows increasing the total device periphery per gain stage significantly.

3. The ability to increase the device periphery makes it possible to bring the optimum ac load line of the FET closer to the output drain line impedance.

4. The capacitors added in series with the gate inputs can each be made different. Thus it is possible to vary the amount of rf voltage sampled from the input line and in this way compensate for the gate line attenuation.

DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

This approach to power amplifier design has been applied to a traveling-wave amplifier in the 2-8 GHz frequency band. The circuit topology is similar to that of in Fig. 1. The design uses six FETs, each with 800 μm gate periphery. Each FET gate is individually biased through 2 KΩ resistors connected to a common gate bias bus. These high-value resistors and the gate and drain line matching resistors are realized using the floating-gate FET resistors shown in Fig. 3. The thin-film capacitors use 0.5 μm thick Si_3N_4 as the dielectric medium. In this way the fabrication process is quite simplified, to no more than the regular FET process plus plasma-assisted chemical vapor deposition of silicon nitride film.

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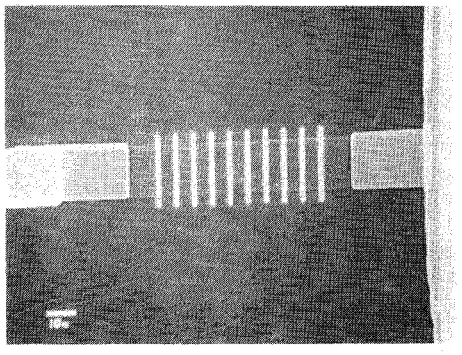

Fig. 3. SEM micrograph of a ten-open-gate FET approximately a 2000 Ω resistor.

The predicted gain and return loss performance of the amplifier is shown in Fig. 4. The gain is very flat and slightly less than 8 dB in the 2-8 GHz design band. The return loss is 12 dB at 2 GHz better than 15 dB above 2.5 GHz.

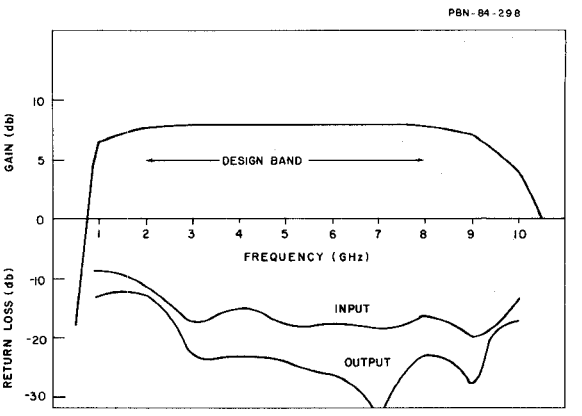

Fig. 4. Predicted performance of the 2-8 GHz amplifier.

The circuit described above has been fabricated on a 100 μm thick GaAs substrate. The finished chip is shown in Fig. 5. Its dimensions are 3 × 3.1 mm. The top plates of the capacitors on the gate pads are proportional to their capacitance. Notice the increase in the area of the top plates as we move along the gate line away from the input terminal. This increase compensates for the attenuation of the gate line. With this approach, we were able to double the maximum allowed gate periphery and quadruple the maximum input power.

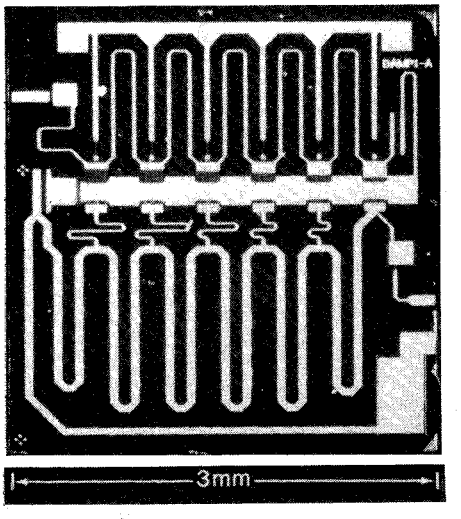

Fig. 5. The finished chip.

Typical small-signal measured performance of the amplifier in 0.5 to 10 GHz frequency band is shown in Fig. 6. The gain is lower than the design by 1.2 dB at the low end and by 2.6 dB at the high end of the band. Input and output return loss is very close to predictions. Power performance of the amplifier is shown in Fig. 7. Near 1 dB compression, the power output is 30 ∓ 0.5 dBm with 5 dB of gain across the 2-8 GHz band.

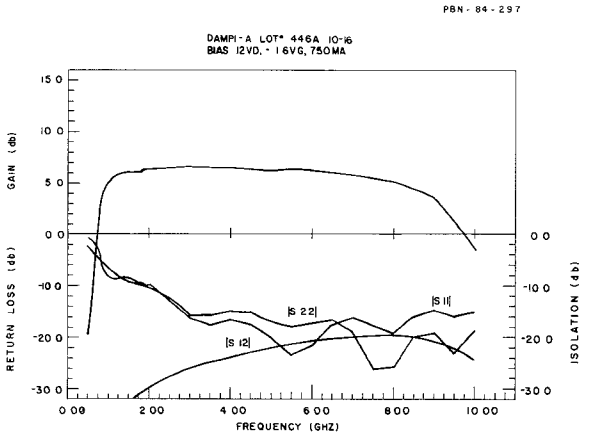

Fig. 6. Small-signal performance of a typical amplifier.

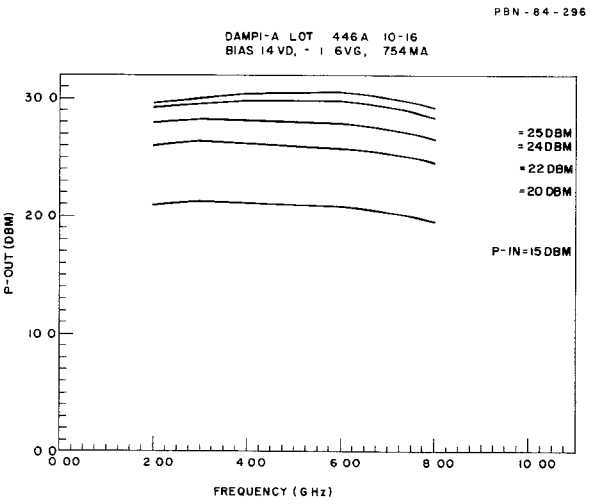

Fig. 7. Measured power performance of the amplifier.

Conclusion

A new circuit approach to increase the power amplification capability of distributed or traveling-wave amplifiers has been introduced. The validity of the approach has been demonstrated by designing a 1 W amplifier in the 2-8 GHz frequency band.

References

[1] Y. Ayasli, L.D. Reynolds, R.L. Mozzi, L.K. Hanes, "2-20 GHz Traveling-Wave Power Amplifier," IEEE Trans. Microwave Theory Tech., vol. MTT-32, (March 1984).